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Published in:
I E E E Transactions on Power Electronics

DOI (link to publication from Publisher):
[10.1109/TPEL.2019.2918271](https://doi.org/10.1109/TPEL.2019.2918271)

Publication date:
2020

Document Version
Accepted author manuscript, peer reviewed version

[Link to publication from Aalborg University](#)

Citation for published version (APA):
Liu, D., Wang, Y., Deng, F., & Chen, Z. (2020). Balanced Power Device Currents Based Modulation Strategy for Full-Bridge Three-Level DC/DC Converter. *I E E E Transactions on Power Electronics*, 35(2), 2008-2022. [8720005]. <https://doi.org/10.1109/TPEL.2019.2918271>

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Balanced Power Device Currents Based Modulation Strategy for Full-Bridge Three-Level (FBTL) DC/DC Converter

Dong Liu, *Member, IEEE*, Yanbo Wang, *Member, IEEE*, Fujin Deng, *Member, IEEE*, and Zhe Chen, *Fellow, IEEE*

Abstract - This paper proposes a new modulation strategy with balanced power device currents for the full-bridge three-level (FBTL) DC/DC converter. The proposed modulation strategy has two working patterns, which can not only realize zero-voltage switching (ZVS) but also satisfy the wide input voltage range. More significantly, the two working patterns of the proposed strategy can both balance the currents among the power switches and clamping diodes in comparison with the conventional control strategies causing current imbalances among the power switches and clamping diodes. Consequently, the proposed strategy can balance the thermal stresses among the power switches and clamping diodes, which would thus improve the converter's reliability. Finally, the experimental results, obtained by a built 1.5 kW experimental prototype, verify almost zero current difference and zero thermal stress difference among the inner power switches, outer power switches, and clamping diodes under the proposed strategy.

Keywords - balanced power device currents, full-bridge three-level (FBTL) DC/DC converter, wide input voltage range, zero-voltage switching (ZVS).

I. INTRODUCTION

The three-level (TL) DC/DC converter is attractive for the high voltage applications, such as three-phase power factor correction systems, renewable energy systems, electric vehicle charging systems, and distributed power systems [1-5], because the voltage stresses on the power switches are only half of the input voltage ($V_{in}/2$) in the TL DC/DC converter [6], [7]. So far, many studies about the TL DC/DC converter have been carried out [8-20]. In [8], a zero-voltage and zero-current switching half-bridge (HB) TL DC/DC converter was proposed, in which the phase-shift control strategy can be applied into the TL DC/DC converter by adding a flying capacitor in the primary side. Based on [8], a TL DC/DC converter with the auxiliary circuit was proposed to reduce the circulating current for the converter's efficiency improvement

[9]. An improved zero-voltage switching (ZVS) DC/DC converter with series-connected transformers was proposed in [10], which can both realize the ZVS within nearly entire load range and balance the output currents. In [11], a novel ZVS TL DC/DC converter was proposed, which features a simple and compact circuit structure by removing two clamped diodes and connecting the mid-points of the input capacitors and switching pairs. Based on [11], four types of new pulse-wide modulation PWM TL DC/DC converters with the wide range soft-switching are proposed for industrial applications in [12] and a new ZVS modulation strategy with input capacitors' current balancing control strategy was proposed in [13] for the TL DC/DC converter. Additionally, a secondary-side phase-shift-controlled ZVS DC/DC converter with the wide voltage gain was proposed in [14] for the high voltage applications, which can effectively reduce the circulating current.

The above studies mainly focus on the HB TL DC/DC converters, but they are not suitable for the high power electronic systems because of the higher current stresses on the power switches in comparison with the full-bridge (FB) DC/DC converters [21-23]. In addition, the modulation strategy of the FB circuit structure is different from that of the HB circuit structure and even more complex due to more power devices in comparison with the HB circuit structure. In [15] and [16], two hybrid ZVS full-bridge three-level (FBTL) DC/DC converters were proposed for high power applications, which are both composed of a TL leg and a two-level leg in the primary side. A zero-voltage and zero-current switching FBTL with reduced circulating current and an improved FBTL DC/DC converter with input capacitors' voltage balancing control strategy were proposed in [17] and [18] respectively, but they cannot satisfy the wide input voltage range. Two modulation strategies named chopping phase-shift (CPS) strategy and double phase-shift (DPS) strategy were proposed in [19] and [20] respectively for the FBTL DC/DC converter, which can both satisfy the wide input voltage range.

When it comes to the modulation strategies for FBTL DC/DC converters, there are mainly three objectives that previous research aims to achieve, which include the soft switching, wide input voltage range, and reliability of input capacitors (capacitors' voltages and currents balancing methods). However, there are few studies paying attention on the current balancing among the power devices in the FBTL

Manuscript received xx. xx, 2018; revised xx. xx, 2018; accepted xx. xx, 2019. Date of current version xx. xx, 2018. This work was supported by the ForsKEL and EUDP project "Voltage control and protection for a grid towards 100% power electronics and cable network (COPE) (No. 64017-0047)". (Corresponding author: Dong Liu.)

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DC/DC converter, which is closely related with the reliability of the converter because the unbalanced currents among the power devices would result in the power loss imbalances and thermal stress imbalances among the power devices [24-26].

In this paper, the current imbalance issue of the power devices under the conventional modulation strategies in the FBTL DC/DC converter is pointed out and analysed in detailed. Then, a new modulation strategy is proposed for the FBTL DC/DC converter to eliminate these current imbalances. In addition, the proposed strategy is composed of two working patterns for satisfying the wide input voltage range. These two working patterns can both realize zero-voltage switching (ZVS) and has the ability of seamless transition. More importantly, the two working patterns can both balance the currents among power switches and clamping diodes. Accordingly, the proposed strategy would balance the power losses and thermal stresses among the power switches and clamping diodes, which is helpful for improving the reliability of the converter. The performances of the FBTL DC/DC converter under the proposed strategy are analysed in detail and verified by the experimental results.

This paper is organized as follows. Section II analyzes the current imbalance issue of the power devices under the conventional strategies. Section III introduces the proposed modulation strategy and analyzes the operation principles of the proposed strategy in detail. Section IV presents the detailed analysis about the characteristics and performances of the proposed strategy. Section V demonstrates the experimental results to verify the proposed strategy. Finally, the main contributions of this paper are summarized in Section VI.

II. CURRENT IMBALANCE ISSUE UNDER CONVENTIONAL STRATEGIES

Fig. 1 shows the circuit structure of the FBTL DC/DC converter.

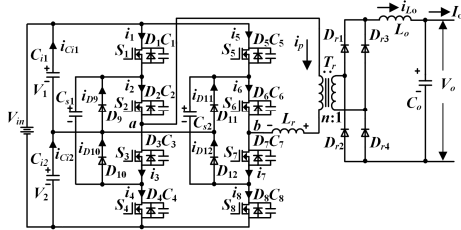


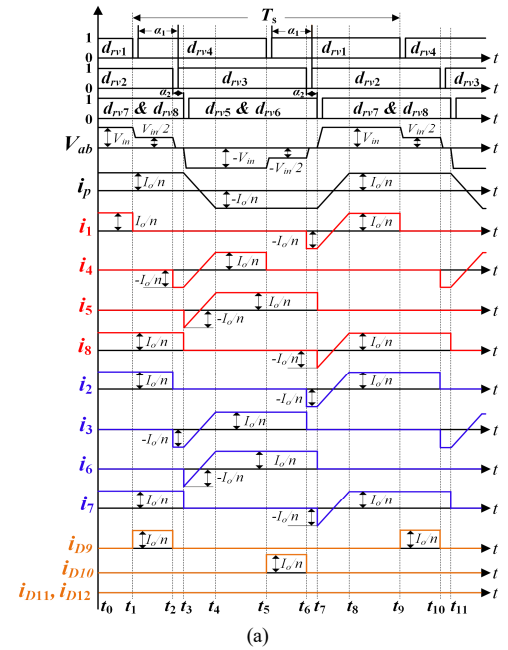
Fig. 1. Circuit Structure of FBTL DC/DC converter.

In Fig. 1, in the primary side, C_{i1} and C_{i2} are two input capacitors which split the input voltage V_{in} into V_1 and V_2 ; S_1, S_4, S_5, S_8 are outer switches and D_1, D_4, D_5, D_8 are their body or paralleled diodes; S_2, S_3, S_6, S_7 are inner power switches and D_2, D_3, D_6, D_7 are their body or paralleled diodes; $C_1 - C_8$ are parasitic capacitors of $S_1 - S_8$; C_{s1} and C_{s2} are two flying capacitors; $D_9 - D_{12}$ are four clamping diodes; T_r is the isolation transformer; L_r is the leakage inductor of T_r plus added inductor in series with T_r . In the secondary side, $D_{r1} - D_{r4}$ are four output rectifier diodes; L_o and C_o are output filter

inductor and output filter capacitor, respectively. In addition, V_{in} is the input voltage; V_1 and V_2 are the voltage on the input capacitor C_{i1} and C_{i2} ; i_{C11} and i_{C12} are the current on the input capacitor C_{i1} and C_{i2} ; V_{ab} is the voltage between the point a and b ; i_p is the primary current of the transformer T_r ; $i_1 - i_8$ are currents on the primary power switches (S_1, D_1) - (S_8, D_8); $i_{D9} - i_{D12}$ are currents on the clamping diodes $D_9 - D_{12}$; n is the turns ratio of the transformer T_r ; i_{Lo} is the current through the output filter inductor L_o ; V_o and I_o are the output voltage and output current respectively.

In order to simplify the following analysis, several assumptions are made as: 1) all the switches and diodes are ideal; 2) two input capacitors C_{i1} and C_{i2} are large enough to be considered as two voltage sources with the values of the half of input voltage ($V_{in}/2$); 3) two flying capacitors C_{s1} and C_{s2} are considered as two voltage sources with the values of $V_{in}/2$ but only provide charging and discharging paths for the switches' parasitic capacitors; 4) the output filter inductor L_o is large enough to be considered as a constant current source; and 5) the parasitic capacitors of $S_1 - S_8$ are the same, which means $C_1 = C_2 = C_3 = C_4 = C_5 = C_6 = C_7 = C_8 = C_j$.

Fig. 2 presents the currents through the power switches ($i_1 - i_8$) and currents through the clamping diodes ($i_{D9} - i_{D12}$) under the DPS strategy as an example to explain the current imbalance issue under the conventional modulation strategies, in which $d_{rv1} - d_{rv8}$ are driving signals for the power switches $S_1 - S_8$; T_s is one switching period; α_1, α_2 , and θ are phase-shift delays. It needs to be mentioned that the currents $i_1 - i_8$ and $i_{D9} - i_{D12}$ under the CPS strategy are the same as that under the DPS strategy.



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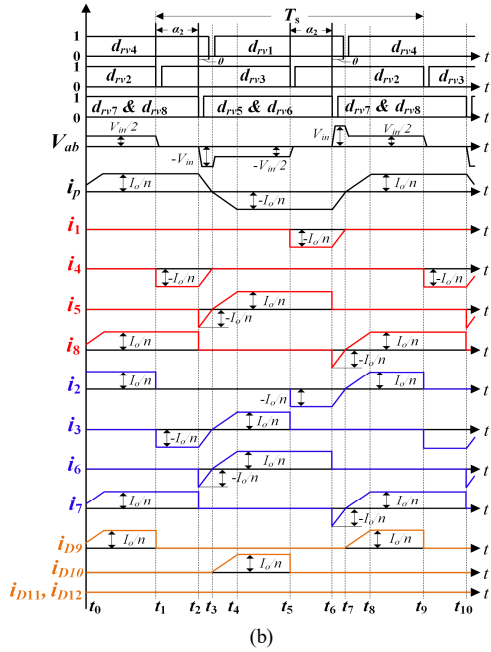


Fig. 2. Currents on primary power devices under DPS strategy. (a) Three-level mode. (b) Two-level mode.

From Fig. 2, it can be observed that: 1) for the currents on the outer power switches (i_1, i_4, i_5, i_8) as marked by red color, i_1, i_4 are the same besides 180° phase difference, i_5, i_8 are the

same besides 180° phase difference, and i_5, i_8 are higher than i_1, i_4 ; 2) for the currents on the inner power switches (i_2, i_3, i_6, i_7) as marked by blue color, i_2, i_3 are the same besides 180° phase difference, i_6, i_7 are the same besides 180° phase difference, the root mean square (RMS) value of i_2, i_3, i_6, i_7 are the same but the average value of i_2, i_3 are smaller than that of i_6, i_7 ; 3) for the currents on the clamping diodes ($i_{D9}, i_{D10}, i_{D11}, i_{D12}$) as marked by orange color, i_{D9}, i_{D10} are the same besides 180° phase difference, i_{D11}, i_{D12} are zero, so i_{D9}, i_{D10} are higher than i_{D11}, i_{D12} . Therefore, based on the above analysis, it can be concluded that the currents among the outer power switches (i_1, i_4, i_5, i_8), inner power switches (i_2, i_3, i_6, i_7), and clamping diodes ($i_{D9}, i_{D10}, i_{D11}, i_{D12}$) are unbalanced under the conventional strategies.

Table I presents the calculation equations about the RMS and average values of $i_1 - i_8$ and $i_{D9} - i_{D12}$ under the DPS strategy according to Fig. 2.

III. PROPOSED MODULATION STRATEGY

In order to eliminate the current imbalances among the power devices under the conventional strategies, a new modulation strategy with balanced power device currents is proposed for FBTL DC/DC converter.

TABLE I. THEORETICAL EQUATIONS ABOUT RMS AND AVERAGE VALUES OF CURRENTS ON PRIMARY POWER DEVICES UNDER DPS STRATEGY

		Three-level mode	Two-level mode
i_1, i_4	RMS value	$\sqrt{\frac{I_o^2 \cdot (T_s - 2 \cdot \alpha_1)}{2 \cdot n^2 \cdot T_s} - \frac{4 \cdot L_r \cdot I_o^3}{3 \cdot V_m \cdot n^3 \cdot T_s}}$	$\sqrt{\frac{I_o^2 \cdot \alpha_2}{n^2 \cdot T_s} + \frac{L_r \cdot I_o^3}{3 \cdot V_m \cdot n^3 \cdot T_s}}$
	Average value	$\frac{I_o \cdot (T_s - 2 \cdot \alpha_1 - 4 \cdot \alpha_2)}{2 \cdot n \cdot T_s} - \frac{2 \cdot L_r \cdot I_o^2}{V_m \cdot n^2 \cdot T_s}$	$-\frac{I_o \cdot \alpha_2}{n \cdot T_s} - \frac{L_r \cdot I_o^2}{2 \cdot V_m \cdot n^2 \cdot T_s}$
i_5, i_8	RMS value	$\sqrt{\frac{I_o^2}{2 \cdot n^2} - \frac{4 \cdot L_r \cdot I_o^3}{3 \cdot V_m \cdot n^3 \cdot T_s}}$	$\sqrt{\frac{I_o^2}{2 \cdot n^2} - \frac{2 \cdot L_r \cdot I_o^3}{V_m \cdot n^3 \cdot T_s}}$
	Average value	$\frac{I_o}{2 \cdot n} - \frac{2 \cdot L_r \cdot I_o^2}{V_m \cdot n^2 \cdot T_s}$	$\frac{I_o}{2 \cdot n} - \frac{5 \cdot L_r \cdot I_o^2}{2 \cdot V_m \cdot n^2 \cdot T_s}$
i_2, i_3	RMS value	$\sqrt{\frac{I_o^2}{2 \cdot n^2} - \frac{4 \cdot L_r \cdot I_o^3}{3 \cdot V_m \cdot n^3 \cdot T_s}}$	$\sqrt{\frac{I_o^2}{2 \cdot n^2} - \frac{2 \cdot L_r \cdot I_o^3}{V_m \cdot n^3 \cdot T_s}}$
	Average value	$\frac{I_o \cdot (T_s - 4 \cdot \alpha_2)}{2 \cdot n \cdot T_s} - \frac{2 \cdot L_r \cdot I_o^2}{V_m \cdot n^2 \cdot T_s}$	$\frac{I_o \cdot (T_s - 4 \cdot \alpha_2)}{2 \cdot n \cdot T_s} - \frac{5 \cdot L_r \cdot I_o^2}{2 \cdot V_m \cdot n^2 \cdot T_s}$
i_6, i_7	RMS value	$\sqrt{\frac{I_o^2}{2 \cdot n^2} - \frac{4 \cdot L_r \cdot I_o^3}{3 \cdot V_m \cdot n^3 \cdot T_s}}$	$\sqrt{\frac{I_o^2}{2 \cdot n^2} - \frac{2 \cdot L_r \cdot I_o^3}{V_m \cdot n^3 \cdot T_s}}$
	Average value	$\frac{I_o}{2 \cdot n} - \frac{2 \cdot L_r \cdot I_o^2}{V_m \cdot n^2 \cdot T_s}$	$\frac{I_o}{2 \cdot n} - \frac{5 \cdot L_r \cdot I_o^2}{2 \cdot V_m \cdot n^2 \cdot T_s}$
i_{D9}, i_{D10}	RMS value	$\frac{I_o}{n} \sqrt{\alpha_1}$	$\sqrt{\frac{I_o^2 \cdot (T_s - 2 \cdot \alpha_1)}{2 \cdot n^2 \cdot T_s} - \frac{7 \cdot L_r \cdot I_o^3}{3 \cdot V_m \cdot n^3 \cdot T_s}}$
	Average value	$\frac{I_o \cdot \alpha_1}{n \cdot T_s}$	$\frac{I_o \cdot (T_s - 2 \cdot \alpha_1)}{2 \cdot n \cdot T_s} - \frac{2 \cdot L_r \cdot I_o^2}{V_m \cdot n^2 \cdot T_s}$
i_{D11}, i_{D12}	RMS value	0	0
	Average value	0	0

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Reference [13] had proposed a similar current balancing method, but it is for the HB TL DC/DC converter. Comparing between the HB and FB TL DC/DC converter, the FBTL DC/DC is more suitable for the high power applications and the modulation strategies between HB and FB TL DC/DC converter are quite different. The modulation strategy of the FBTL DC/DC converter is more complex than that of the HB TL DC/DC converter not only because the circuit structure of the FB converter is more complex but also because the modulation strategy for the FBTL DC/DC converter normally needs to satisfy the wide input voltage range. In order to satisfy the wide input voltage range, the proposed modulation strategy is composed of two working patterns. More significantly, these two working patterns can both effectively balance the currents among the power devices and the transition between these two working patterns is seamless.

Figs. 3(a) and 3(b) show the operation principles of two working patterns respectively, in which $d_{rv1} - d_{rv8}$ are driving signals of the power switches $S_1 - S_8$; d_1 and d_2 are duty ratios in one switching period T_s .

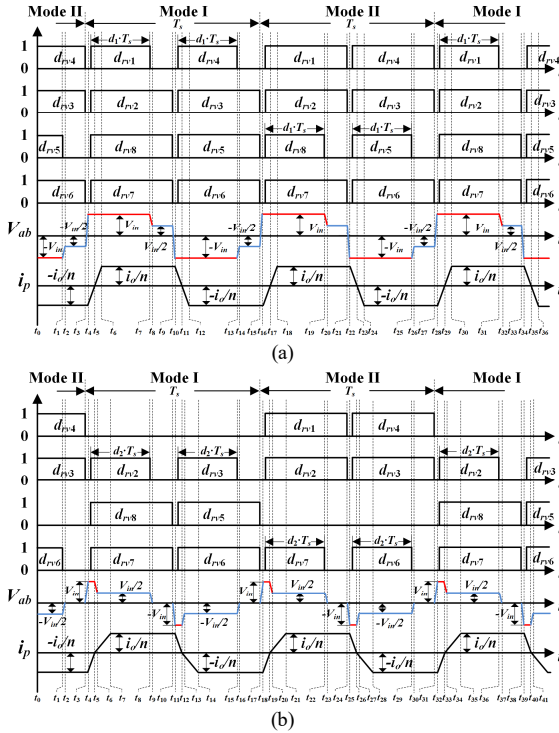


Fig. 3. Proposed modulation strategy. (a) Working pattern I. (b) Working pattern II.

1) *Working pattern I* is used for the low input voltage. In the working pattern I, the output voltage V_o is adjusted by changing the duty ratio d_1 . The working pattern I operates by swapping the duty ratios for the switching pairs (S_1, S_8) and (S_4, S_5) respectively in every switching period to make the currents through the power devices balanced in every two switching periods. Therefore, the working pattern I has two operation modes as marked in Fig. 3(a) that: in the mode I as $[t_3 - t_{15}]$, the duty ratio of d_{rv1} and d_{rv4} are both d_1 , the duty ratio of d_{rv2} , d_{rv3} , d_{rv5} , d_{rv6} , d_{rv7} , and d_{rv8} are all 0.5 if neglecting the dead

time; but in the mode II as $[t_{15} - t_{27}]$, the duty ratio of d_{rv5} and d_{rv8} are both d_1 , the duty ratio of d_{rv1} , d_{rv2} , d_{rv3} , d_{rv4} , d_{rv6} , and d_{rv7} are all 0.5 if neglecting the dead time. By adjusting the value of d_1 , the time length of the third-level voltages (V_{in} and $-V_{in}$) as marked by red color in Fig. 3(a) can be changed, which would thus change the output voltage V_o . For instance, if reducing d_1 , the time length of the third-level voltages (V_{in} and $-V_{in}$) would decrease, which means that the output voltage V_o would decrease.

2) *Working pattern II* is used for the high input voltage when d_1 reduces to zero. In the working pattern II, the output voltage V_o is adjusted by changing the duty ratio d_2 . The working pattern II operates by swapping the duty ratios for the switching pairs (S_1, S_8), (S_2, S_7), (S_3, S_6), and (S_4, S_5) respectively in every switching period to balance the currents through the power devices in every two switching periods. Therefore, the working pattern II also has two operation modes as marked in Fig. 3(b) that: in the mode I as $[t_3 - t_{17}]$, the duty ratios of d_{rv1} and d_{rv4} are both 0, the duty ratio of d_{rv2} and d_{rv3} are both d_2 , and the duty ratio of d_{rv5} , d_{rv6} , d_{rv7} , and d_{rv8} are all 0.5 if neglecting the dead time; but in the mode II as $[t_{17} - t_{31}]$, the duty ratio of d_{rv5} and d_{rv8} are both 0, the duty ratio of d_{rv6} and d_{rv7} are both d_2 , and the duty ratio of d_{rv1} , d_{rv2} , d_{rv3} , and d_{rv4} are all 0.5 if neglecting the dead time. By adjusting the value of d_2 , the time length of the second-level voltages ($V_{in}/2$ and $-V_{in}/2$) as marked by blue color in Fig. 3(b) can be changed, which would thus change the output voltage V_o . For instance, if reducing d_2 , the time length of the second-level voltages ($V_{in}/2$ and $-V_{in}/2$) would decrease, which means that the output voltage V_o would decrease.

Fig. 4 presents the equivalent circuits of the working pattern I shown in Fig. 3(a) as an example to analyze the operation principle of the proposed strategy. The analysis of the operation principle in the working pattern II is similar to that in the working pattern I, which is not repeated here.

Stage 1 [before t_3]: The power switches S_3, S_4 , and S_6 are all in on-state, so the primary voltage V_{ab} equals to $-V_{in}/2$ and the input power transfers to the load from D_{r2} and D_{r3} . The primary current of the transformer i_p is $-I_o/n$.

Stage 2 [$t_3 - t_4$]: At t_3 , the power switches S_3, S_4 , and S_6 are turned off. Then the parasitic capacitors C_3, C_4, C_6 are charged and C_1, C_2, C_7 are discharged. The primary current i_p starts to increase and is not enough to provide output current, so the output rectifier diodes D_{r1}, D_{r2}, D_{r3} , and D_{r4} conduct simultaneously, which clamps both the primary and secondary voltage of the transformer at 0 V.

Stage 3 [$t_4 - t_5$]: At t_4 , the voltages on C_3, C_4, C_6 increase to $V_{in}/2$ and the voltages on C_1, C_2, C_7 decrease to 0 V, so the primary voltage V_{ab} reaches to V_{in} . Then the primary current i_p flows through D_{r1}, D_{r2}, D_{r7} , and D_{r8} , which clamps the voltage on S_1, S_2, S_7 , and S_8 at 0 V. Therefore, S_1, S_2, S_7 , and S_8 can be turned on with zero-voltage. During this time period, the primary current i_p increases linearly because the voltage on L_r is the input voltage V_{in} .

Stage 4 [$t_5 - t_6$]: At t_5 , the primary current i_p increases to 0 A, which means the current direction of i_p would change. During

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this time period, the primary current i_p still increases linearly because the voltage on L_r maintains V_{in} .

Stage 5 $[t_6 - t_7]$: At t_6 , the primary current i_p increases to the positive reflected output current whose value is I_o/n . Then the output rectifier diodes D_{r2} and D_{r3} are turned off, and the input power would transfer to load from D_{r1} and D_{r4} .

Stage 6 $[t_7 - t_8]$: At t_7 , the power switch S_1 is turned off. Then the parasitic capacitor C_1 is charged and C_4 is discharged.

Stage 7 $[t_8 - t_9]$: At t_8 , the voltage on C_1 increases to $V_{in}/2$ and the voltage on C_4 decreases to 0 V. Then, the clamping diode D_9 conducts and the primary current i_p flows through D_9 , S_2 , S_7 , and S_8 . During this time period, the primary voltage V_{ab} is $V_{in}/2$.

At t_9 , the power switches S_2 , S_7 , and S_8 are turned off. The second half cycle $[t_9 - t_{15}]$ of the mode I starts, whose analysis is similar to the first half cycle $[t_3 - t_9]$. The analysis of the mode II is similar to that of the mode I, which is not repeated here.

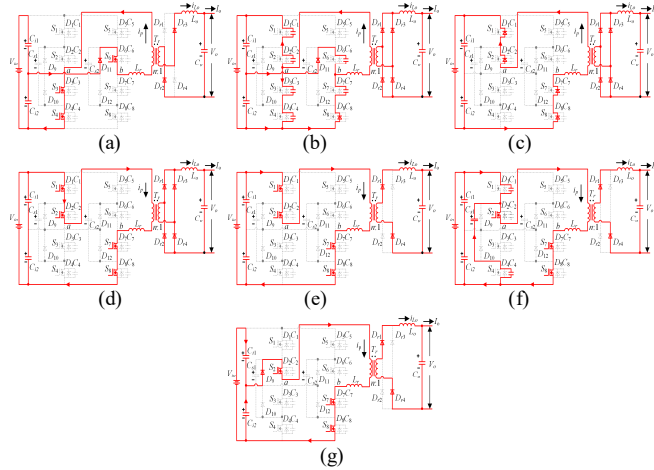


Fig. 4. Equivalent circuits under working pattern I of proposed strategy. (a) [before t_3]. (b) $[t_3-t_4]$. (c) $[t_4-t_5]$. (d) $[t_5-t_6]$. (e) $[t_6-t_7]$. (f) $[t_7-t_8]$. (g) $[t_8-t_9]$.

IV. CHARACTERISTICS AND PERFORMANCES OF PROPOSED STRATEGY

A. Duty Cycle Loss

In the working pattern I shown in Fig. 3(a), $[t_3 - t_6]$, $[t_9 - t_{12}]$ and $[t_{15} - t_{18}]$, $[t_{21} - t_{24}]$ are the time intervals of the duty cycle loss in the mode I and II respectively, and these four time intervals are the same. If neglecting the quite short time intervals $[t_3 - t_4]$, $[t_9 - t_{10}]$, $[t_{15} - t_{16}]$, and $[t_{21} - t_{22}]$, they can be calculated by (1).

$$t_6 - t_3 = t_{12} - t_9 = t_{18} - t_{15} = t_{24} - t_{21} = \frac{2 \cdot L_r \cdot I_o}{n \cdot V_{in}} \quad (1)$$

Based on (1), the duty cycle loss in every switching period T_s under the working pattern I namely d_{loss_I} can be obtained by (2).

$$d_{loss_I} = \frac{t_6 - t_3}{T_s} = \frac{t_{12} - t_9}{T_s} = \frac{t_{18} - t_{15}}{T_s} = \frac{t_{24} - t_{21}}{T_s} = \frac{2 \cdot L_r \cdot I_o}{n \cdot V_{in} \cdot T_s} \quad (2)$$

In the working pattern II shown in Fig. 3(b), $[t_3 - t_7]$, $[t_{10} - t_{14}]$ and $[t_{17} - t_{21}]$, $[t_{24} - t_{28}]$ are the time intervals of the duty cycle loss in the mode I and II respectively, and these four time intervals are the same. If neglecting the quite short time intervals $[t_3 - t_4]$, $[t_{10} - t_{11}]$, $[t_{17} - t_{18}]$, and $[t_{24} - t_{25}]$, they can be calculated by (3).

$$t_7 - t_3 = t_{14} - t_{10} = t_{21} - t_{17} = t_{28} - t_{24} = \frac{3 \cdot L_r \cdot I_o}{n \cdot V_{in}} \quad (3)$$

Based on (3), the duty cycle loss in every switching period T_s under the working pattern II namely d_{loss_II} can be obtained by (4).

$$d_{loss_II} = \frac{t_7 - t_3}{T_s} = \frac{t_{14} - t_{10}}{T_s} = \frac{t_{21} - t_{17}}{T_s} = \frac{t_{28} - t_{24}}{T_s} = \frac{3 \cdot L_r \cdot I_o}{n \cdot V_{in} \cdot T_s} \quad (4)$$

Table II presents the comparison results about the duty cycle loss under the conventional strategies and proposed strategy. From Table II, it can be observed that: 1) the duty cycle loss of the working pattern I under the proposed strategy is smaller than that of the three-level mode under the conventional strategies; 2) The duty cycle loss of the working pattern II under the proposed strategy is the same as that of the two-level mode under the CPS strategy.

B. Output Characteristics

If neglecting the effect of the dead time, the average output voltage in the working pattern I namely V_{o_I} and working pattern II namely V_{o_II} can be calculated by (5) and (6), respectively.

$$V_{o_I} = \frac{2 \cdot \left[\int_0^{(d_1 - d_{loss_I})T_s} \frac{V_{in}}{n} + \int_0^{(0.5 - d_1)T_s} \frac{V_{in}}{2 \cdot n} \right]}{T_s} \quad (5)$$

$$= \frac{V_{in}}{n} \cdot (0.5 + d_1 - 2 \cdot d_{loss_I}) = \frac{V_{in}}{n} \cdot (0.5 + d_1 - \frac{4 \cdot L_r \cdot I_o}{n \cdot V_{in} \cdot T_s})$$

$$V_{o_II} = \frac{2 \cdot \left[\int_0^{(d_2 - d_{loss_II})T_s} \frac{V_{in}}{2 \cdot n} \right]}{T_s} = \frac{V_{in}}{n} \cdot (d_2 - d_{loss_II}) = \frac{V_{in}}{n} \cdot (d_2 - \frac{3 \cdot L_r \cdot I_o}{n \cdot V_{in} \cdot T_s}) \quad (6)$$

C. ZVS Achievement Conditions

1) Working Pattern I

In the mode I, the zero-voltage switch-on of the power switches S_4 and S_8 is mainly determined by the reflected current from the output filter inductor. Normally, the output filter inductance is quite large enough to make the power switches S_4 and S_8 achieve zero-voltage switch-on even at the light load. For instance, in order to ensure the zero-voltage switch-on of the power switch S_4 in Fig. 3(a), the energy E_1 is needed to discharge the capacitor C_4 from $V_{in}/2$ to 0 V and charge the capacitor C_1 from 0 V to $V_{in}/2$, whose expression can be given by (7).

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TABLE II. COMPARISON RESULTS ABOUT DUTY CYCLE LOSS

Item		CPS Strategy	DPS Strategy	Proposed Strategy
Duty Cycle Loss	Three-level mode/ Working pattern I	$\frac{4 \cdot L_r \cdot I_o}{n \cdot V_m \cdot T_s} + \frac{2 \cdot \theta}{T_s}$	$\frac{4 \cdot L_r \cdot I_o}{n \cdot V_m \cdot T_s} + \frac{2 \cdot \theta}{T_s}$	$\frac{4 \cdot L_r \cdot I_o}{n \cdot V_m \cdot T_s}$
	Two-level mode/ Working pattern II	$\frac{6 \cdot L_r \cdot I_o}{n \cdot V_m \cdot T_s}$	$\frac{8 \cdot L_r \cdot I_o}{n \cdot V_m \cdot T_s} - \frac{2 \cdot \alpha}{T_s}$	$\frac{6 \cdot L_r \cdot I_o}{n \cdot V_m \cdot T_s}$

Note: θ is the phase shift time between the driving signals of S_2 and (S_7, S_8) or the driving signals S_3 and (S_5, S_6) in the CPS and DPS strategy. α is a constant overlap time between the driving signals of S_1 and (S_7, S_8) or the driving signals S_4 and (S_5, S_6) in the DPS strategy.

$$E_1 \geq \frac{1}{2} \cdot C_1 \cdot \left(\frac{V_{in}}{2}\right)^2 + \frac{1}{2} \cdot C_4 \cdot \left(\frac{V_{in}}{2}\right)^2 = \frac{1}{4} \cdot C_j \cdot V_{in}^2 \quad (7)$$

In the mode I, the energy stored in the inductor L_r is used to realize the zero-voltage switch-on for the power switches S_1, S_2, S_3, S_5, S_6 , and S_7 . For instance, in order to achieve the zero-voltage switch-on for the power switches S_3, S_5 , and S_6 in Fig. 3(a), the capacitors C_3, C_5, C_6 need to be discharged from $V_{in}/2$ to 0 V and the capacitors C_2, C_7, C_8 need to be charged from 0 V to $V_{in}/2$. Accordingly, the following equation (8) should be satisfied to achieve the zero-voltage switch-on of S_3, S_5 , and S_6 .

$$\frac{1}{2} L_r \cdot \left(\frac{I_o}{n}\right)^2 \geq \frac{1}{2} \cdot (C_1 + C_2 + C_3 + C_5 + C_6 + C_7) \cdot \left(\frac{V_{in}}{2}\right)^2 = \frac{3}{4} \cdot C_j \cdot V_{in}^2 \quad (8)$$

In the mode II, the reflected current from the output filter inductor is used to realize the zero-voltage switch-on for the power switches S_1 and S_5 ; and the energy stored in the inductor L_r is used to realize the zero-voltage switch-on for the switches S_2, S_3, S_4, S_6, S_7 , and S_8 . The requirements for the power switches to achieve zero-voltage switch-on in the mode II are same as that in the operation mode I, which is not repeated here.

Therefore, based on (8), the load range of ZVS achievement in the working pattern I namely $I_{o_ZVS_I}$ can be obtained by (9).

$$I_{o_ZVS_I} \geq n \cdot V_m \cdot \sqrt{\frac{3 \cdot C_j}{2 \cdot L_r}} \quad (9)$$

2) Working Pattern II

In the mode I, the zero-voltage switch-on of power switches S_3, S_7 and S_8 is mainly determined by the reflected current from the output filter inductor. Normally, the output filter inductance is quiet large enough to make the power switches S_3, S_7 , and S_8 achieve zero-voltage switch-on even at the light load. For instance, in order to ensure the zero-voltage switch-on of the power switch S_3 in Fig. 3(b), the energy E_2 is needed to discharge the capacitor C_3 from $V_{in}/2$ to 0 V and charge the capacitor C_2 from 0 V to $V_{in}/2$, whose expression can be given by (10).

$$E_2 \geq \frac{1}{2} \cdot C_2 \cdot \left(\frac{V_{in}}{2}\right)^2 + \frac{1}{2} \cdot C_3 \cdot \left(\frac{V_{in}}{2}\right)^2 = \frac{1}{4} \cdot C_j \cdot V_{in}^2 \quad (10)$$

In the mode I, the energy stored in the inductor L_r is used to realize the zero-voltage switch-on for the power switches S_2, S_5 , and S_6 . For instance, in order to achieve the zero-voltage switch-on for the power switches S_5 and S_6 in Fig. 3(b), the capacitors C_5, C_6 need to be discharged from $V_{in}/2$ to 0 V and the capacitors C_7, C_8 need to be charged from 0 V to $V_{in}/2$. Accordingly, the following equation (11) should be satisfied to achieve the zero-voltage switch-on of S_5 and S_6 .

$$\frac{1}{2} L_r \cdot \left(\frac{I_o}{n}\right)^2 \geq \frac{1}{2} \cdot (C_5 + C_6 + C_7 + C_8) \cdot \left(\frac{V_{in}}{2}\right)^2 = \frac{1}{2} \cdot C_j \cdot V_{in}^2 \quad (11)$$

In the mode II, the reflected current from the output filter inductor is used to realize the zero-voltage switch-on for the power switches S_1, S_2 , and S_6 ; and the energy stored in the inductor L_r is used to realize the zero-voltage switch-on for the switches S_3, S_4 , and S_7 . The requirements for the power switches to achieve zero-voltage switch-on in the mode II are same as that in the operation mode I, which is not repeated here.

Therefore, based on (11), the load range of ZVS achievement in the working pattern I namely $I_{o_ZVS_II}$ can be obtained by (12).

$$I_{o_ZVS_II} \geq n \cdot V_m \cdot \sqrt{\frac{C_j}{L_r}} \quad (12)$$

Table III presents the comparison results about the ZVS range under the conventional strategies and proposed strategy. From Table III, it can be observed that: 1) the ZVS range of the working pattern II under the proposed strategy is the same as that of the three-level mode under the conventional strategies; 2) the ZVS range of the working pattern I under the proposed strategy is little smaller than that of the three-level mode under the conventional strategies because the conventional strategies could realize the ZVS of one more power switch by increasing the duty cycle loss.

D. Currents on Power Devices

Fig. 5 shows the currents flowing through the primary power devices under the proposed strategy. From Fig. 5, it can be observed that: 1) under the working pattern I, the currents on the outer power switches i_1, i_4, i_5, i_8 , on the inner power switches i_2, i_3, i_6, i_7 , and on the clamping diodes $i_{D9}, i_{D10}, i_{D11}, i_{D12}$ are the same besides phase difference, respectively; 2) under the working pattern II, the RMS and average values of i_1, i_4, i_5, i_8 are the same respectively, the RMS and average values of i_2, i_3, i_6, i_7 are also the same respectively, and $i_{D9}, i_{D10}, i_{D11}, i_{D12}$ are the same besides phase difference. Based on the above analysis, it can be concluded that the two working patterns of the proposed strategy can both balance the currents among the power switches and clamping diodes.

Table IV presents the calculation equations about the RMS and average values of $i_1 - i_8$ and $i_{D9} - i_{D12}$ under the proposed strategy according to Fig. 5.

TABLE III. COMPARISON RESULTS ABOUT ZVS ACHIEVEMENT CONDITIONS

Item			CPS Strategy	DPS Strategy	Proposed Strategy
ZVS Range	Three-level mode/ Working pattern I	$I_0 \geq$	$n \cdot V_m \cdot \sqrt{\frac{C_f}{L_r}}$	$n \cdot V_m \cdot \sqrt{\frac{C_f}{L_r}}$	$n \cdot V_m \cdot \sqrt{\frac{3 \cdot C_f}{2 \cdot L_r}}$
	Two-level mode/ Working pattern II		$n \cdot V_m \cdot \sqrt{\frac{C_f}{L_r}}$	$n \cdot V_m \cdot \sqrt{\frac{C_f}{L_r}}$	$n \cdot V_m \cdot \sqrt{\frac{C_f}{L_r}}$

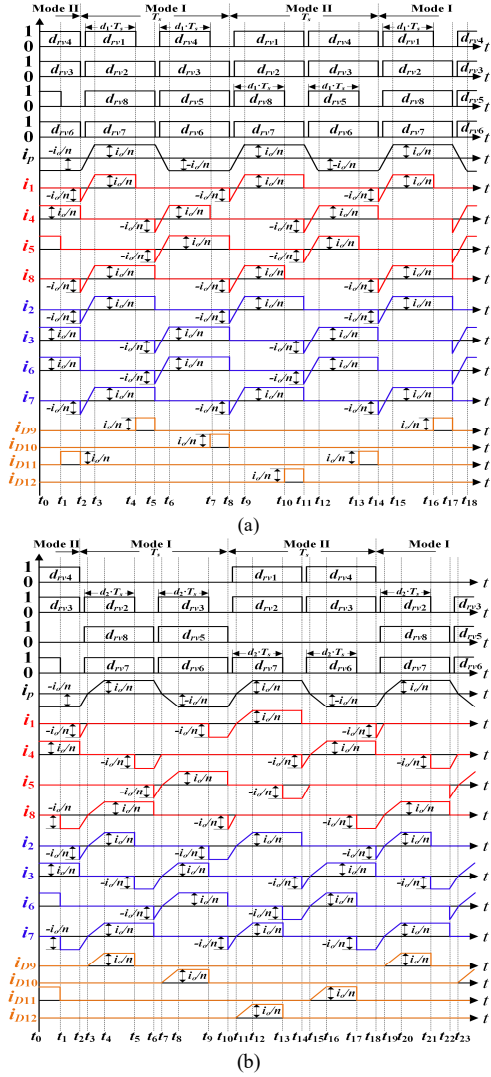


Fig. 5. Currents on primary power devices under proposed strategy. (a) Working pattern I. (b) Working pattern II.

According to the equations in Tables I, IV and circuit parameters in Appendix, the theoretical comparison results about the currents on the primary power devices are presented in Figs. 6 - 8, in which $i_{1_rms_three_DPS} - i_{8_rms_three_DPS}$, $i_{1_avg_three_DPS} - i_{8_avg_three_DPS}$ and $i_{1_rms_two_DPS} - i_{8_rms_two_DPS}$, $i_{1_avg_two_DPS} - i_{8_avg_two_DPS}$ are the RMS value, average value of the currents on the power switches (S_1, D_1) - (S_8, D_8) under the three-level and two-level mode of the DPS strategy respectively; $i_{D9_rms_three_DPS} - i_{D12_rms_three_DPS}$, $i_{D9_avg_three_DPS} - i_{D12_avg_three_DPS}$ and $i_{D9_rms_two_DPS} - i_{D12_rms_two_DPS}$, $i_{D9_avg_two_DPS} - i_{D12_avg_two_DPS}$ are the RMS value, average value of the currents on the clamping diodes $D_9 - D_{12}$ under the three-level and two-level mode of the DPS strategy respectively; $i_{1_rms_I} - i_{8_rms_I}$, $i_{1_avg_I} - i_{8_avg_I}$ and $i_{1_rms_II} - i_{8_rms_II}$, $i_{1_avg_II} - i_{8_avg_II}$ are the RMS value, average value of the currents on the power switches (S_1, D_1) - (S_8, D_8) under the working pattern I and II of the proposed strategy respectively; $i_{D9_rms_I} - i_{D12_rms_I}$, $i_{D9_avg_I} - i_{D12_avg_I}$ and $i_{D9_rms_II} - i_{D12_rms_II}$, $i_{D9_avg_II} - i_{D12_avg_II}$ are the RMS value, average value of the currents on the clamping diodes $D_9 - D_{12}$ under the working pattern I and II of the proposed strategy respectively.

From Figs. 6 - 8, it can be observed that: 1) for the currents on the outer power switches (i_1, i_4, i_5, i_8) in Fig. 6, the RMS and average value of i_5, i_8 are larger than that of i_1, i_4 under the conventional strategy; but the RMS and average value of them become the same under the proposed strategy; 2) for the currents on the inner power switches (i_2, i_3, i_6, i_7) in Fig. 7, the RMS value of them are the same but the average value of i_6, i_7 are larger than that of i_2, i_3 under the conventional strategy; the RMS and average value of them become the same under the proposed strategy; 3) for the currents on the clamping diodes ($i_{D9}, i_{D10}, i_{D11}, i_{D12}$) in Fig. 8, the RMS and average value of i_{D9}, i_{D10} are larger than that of i_{D11}, i_{D12} under the conventional strategy; but the RMS and average value of them become the same under the proposed strategy; 4) the differences among the currents on outer power switches, inner power switches, and clamping diodes under the conventional strategy would become larger with the increasing of the output power.

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TABLE IV. THEORETICAL EQUATIONS ABOUT RMS AND AVERAGE VALUES OF CURRENTS ON PRIMARY POWER DEVICES UNDER PROPOSED STRATEGY

i_1, i_4, i_5, i_8	RMS value	Working pattern I	Working pattern II
		$\sqrt{\frac{I_o^2 \cdot (1+2 \cdot d_1)}{4 \cdot n^2} - \frac{4 \cdot L_r \cdot I_o^3}{3 \cdot V_m \cdot n^3 \cdot T_s}}$	$\sqrt{\frac{I_o^2 \cdot (1-d_2)}{2 \cdot n^2} - \frac{5 \cdot L_r \cdot I_o^3}{6 \cdot V_m \cdot n^3 \cdot T_s}}$
i_2, i_3, i_6, i_7	RMS value	$\sqrt{\frac{I_o^2}{2 \cdot n^2} - \frac{4 \cdot L_r \cdot I_o^3}{3 \cdot V_m \cdot n^3 \cdot T_s}}$	$\sqrt{\frac{I_o^2}{2 \cdot n^2} - \frac{2 \cdot L_r \cdot I_o^3}{V_m \cdot n^3 \cdot T_s}}$
		$\frac{I_o \cdot (1+2 \cdot d_1)}{4 \cdot n} - \frac{2 \cdot L_r \cdot I_o^2}{V_m \cdot n^2 \cdot T_s}$	$\frac{I_o \cdot d_2}{2 \cdot n} - \frac{3 \cdot L_r \cdot I_o^2}{2 \cdot V_m \cdot n^2 \cdot T_s}$
$i_{D9}, i_{D10}, i_{D11}, i_{D12}$	RMS value	$\frac{I_o}{n} \cdot \sqrt{\frac{1-2 \cdot d_1}{4}}$	$\sqrt{\frac{I_o^2 \cdot d_2}{2 \cdot n^2} - \frac{7 \cdot L_r \cdot I_o^3}{6 \cdot V_m \cdot n^3 \cdot T_s}}$
		$\frac{I_o \cdot (1-2 \cdot d_1)}{4 \cdot n}$	$\frac{I_o \cdot d_2}{2 \cdot n} - \frac{L_r \cdot I_o^2}{V_m \cdot n^2 \cdot T_s}$

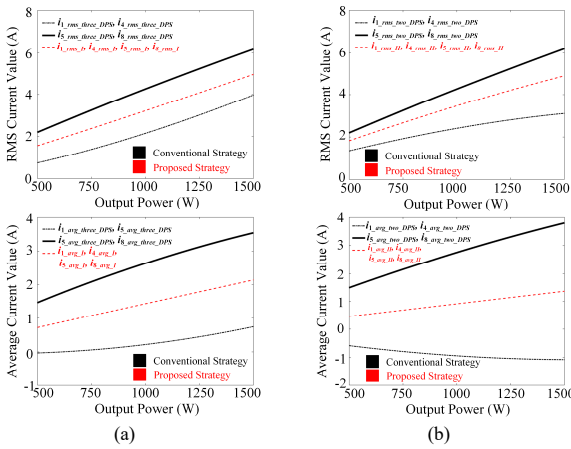


Fig. 6. Theoretical calculation about RMS and average values of currents on outer power switches. (a) Three-level mode of DPS strategy and working pattern I of proposed strategy ($V_{in} = 350$ V, $V_o = 50$ V). (b) Two-level mode of DPS strategy and working pattern II of proposed strategy ($V_{in} = 550$ V, $V_o = 50$ V).

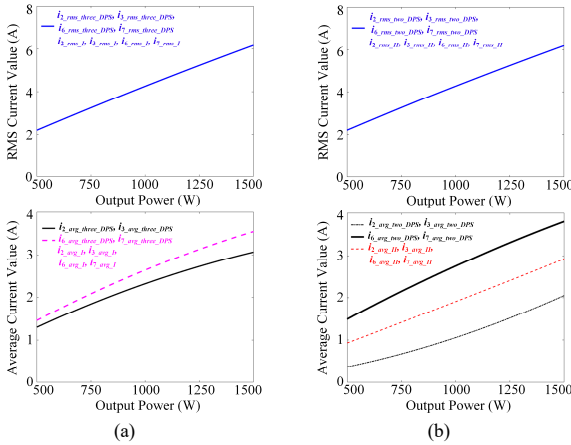


Fig. 7. Theoretical calculation about RMS and average values of currents on inner power switches. (a) Three-level mode of DPS strategy and working pattern I of proposed strategy ($V_{in} = 350$ V, $V_o = 50$ V). (b) Two-level mode of DPS strategy and working pattern II of proposed strategy ($V_{in} = 550$ V, $V_o = 50$ V).

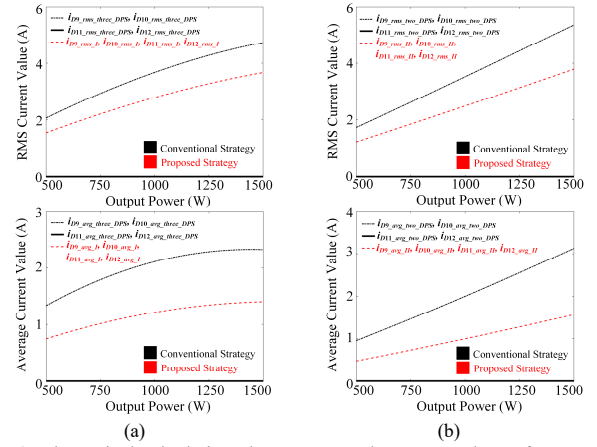


Fig. 8. Theoretical calculation about RMS and average values of currents on clamping diodes. (a) Three-level mode of DPS strategy and working pattern I of proposed strategy ($V_{in} = 350$ V, $V_o = 50$ V). (b) Two-level mode of DPS strategy and working pattern II of proposed strategy ($V_{in} = 550$ V, $V_o = 50$ V).

E. Implementation of Proposed Strategy

For the working pattern I, the duty cycle d_1 calculated by the control loop would be changed in every two switching periods to adjust the output voltage V_o in the practical application. As shown in Fig. 3(a), in the first switching period, the calculated d_1 is set for the driving signals of the power switches S_1, S_4 and the duct cycle 0.5 minus the dead time divided by T_s is set for the driving signals of the power switches S_2, S_3, S_5, S_6, S_7 , and S_8 ; in the second switching period, the calculated d_1 is set for the driving signals of the power switches S_5, S_8 and the duct cycle 0.5 minus the dead time divided by T_s is set for the driving signals of the power switches S_1, S_2, S_3, S_4, S_6 , and S_7 . With the increasing of the input voltage, d_1 would decrease to maintain the output voltage at the constant value. When d_1 reduces to the zero, then the working pattern II starts to be utilized and d_1 is kept at zero, so the transition between the two working patterns is seamless. For the working pattern II, the duty cycle d_2 calculated by the control loop would be changed in every two switching periods to adjust the output voltage V_o in the practical application. As shown in Fig. 3(b), in the first

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switching period, the calculated d_2 is set for the driving signals of the power switches S_2 , S_3 and the duct cycle 0.5 minus the dead time divided by T_s is set for the driving signals of the power switches S_5 , S_6 , S_7 , and S_8 ; in the second switching period, the calculated d_2 is set for the driving signals of the power switches S_6 , S_7 and the duct cycle 0.5 minus the dead time divided by T_s is set for the driving signals of the power switches S_1 , S_2 , S_3 , and S_4 .

Under the steady operations, the duty cycle d_1 and d_2 calculated by the control algorithms are adjusted in every two switching periods to control the output voltage and balance the currents on the primary power devices. Under the dynamic changes, the duty cycle d_1 and d_2 calculated by the control algorithms can be adjusted in every switching period to control the converter, which would thus make dynamic responses as the conventional modulation strategies, because both working pattern I and II have the feature that the mode I and II (shown in Fig. 3) can be utilized alone separately to control the output voltage and have the same output characteristics.

Fig. 9 presents the diagram about the implementation of the proposed modulation strategy, in which the conventional proportional-integral PI control algorithm is utilized to calculate duty cycles d_1 and d_2 . As shown in Fig. 9, the working pattern I is used for the low input voltage by adjusting the duty cycle d_1 from maximum value d_{1max} to 0; when d_1 decreases to 0 due to the increasing of the input voltage, the working pattern II would be used for the higher input voltage by adjusting the duty cycle d_2 .

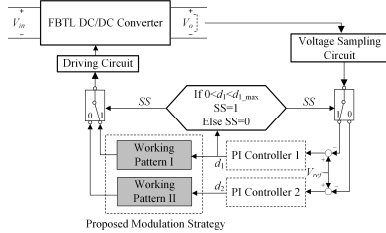


Fig. 9. Diagram about implementation of proposed control strategy.

V. EXPERIMENTAL VERIFICATION

In order to verify the proposed modulation strategy, a 1.5 kW experimental prototype is established, whose circuit parameters are presented in Appendix. Figs. 10(a) and 10(b) present the experimental set-up and hardware of FBTL DC/DC converter.

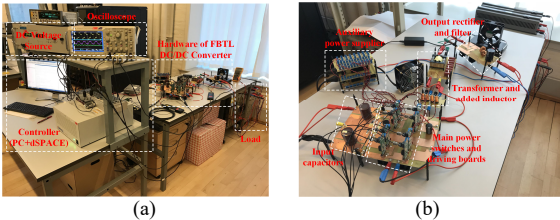


Fig. 10. (a) Experimental set-up. (b) Hardware of FBTL DC/DC converter.

Figs. 11(a) and 10(b) present the experimental results including the primary voltage V_{ab} , output voltage V_o , primary

current i_p , and current through the output filter inductor i_{Lo} under the working pattern I and II.

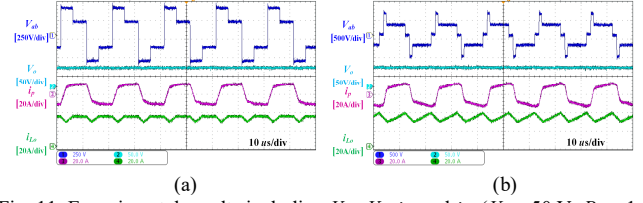


Fig. 11. Experimental results including V_{ab} , V_o , i_p , and i_{Lo} ($V_o = 50$ V, $P_o = 1.5$ kW). (a) Working pattern I of proposed strategy ($V_{in} = 350$ V). (b) Working pattern II of proposed strategy ($V_{in} = 550$ V).

Fig. 12 presents experimental results including the voltages and currents on the input capacitors (V_1 , V_2 , i_{C1} , and i_{C2}) when the output voltage V_o is 50 V and output power P_o is 1.5 kW. From Fig. 12, it can be observed that: under the proposed modulation strategy, 1) the voltages on the input capacitors (V_1 , V_2) are balanced; 2) the currents on the input capacitors (i_{C1} , i_{C2}) are also balanced, and RMS of i_{C1} , i_{C2} under the working pattern I ($V_{in} = 350$ V) and II ($V_{in} = 550$ V) are about 5.1 A and 4.5 A respectively.

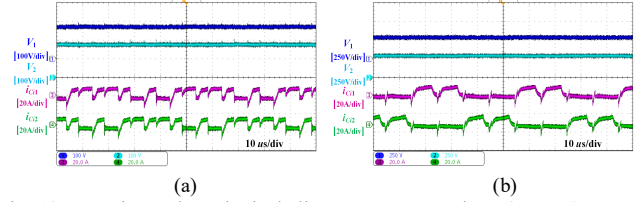
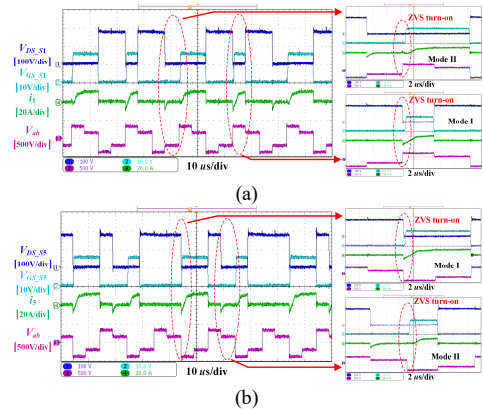


Fig. 12. Experimental results including V_1 , V_2 , i_{C1} , and i_{C2} ($V_o = 50$ V, $P_o = 1.5$ kW). (a) Working pattern I of proposed strategy ($V_{in} = 350$ V). (b) Working pattern II of proposed strategy ($V_{in} = 550$ V).

Figs. 13(a) - 13(c) show the ZVS achievement performances of the power switches S_1 , S_5 , and S_6 under the working pattern I, in which it can be observed that S_1 , S_5 , and S_6 realize zero-voltage switching-on. Figs. 14(a) - 14(b) present the ZVS achievement performances of the power switches S_2 and S_7 under the working pattern II, in which it can be observed that S_2 and S_7 realize zero-voltage switching-on. The ZVS achievement performances of other power switches are similar to the results in Figs. 13 - 14, which are not repeated here.



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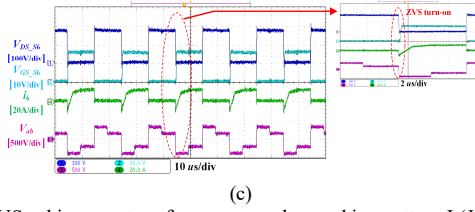


Fig. 13. ZVS achievement performances under working pattern I ($V_{in} = 350$ V, $V_o = 50$ V, $P_o = 1.5$ kW). (a) S_1 . (b) S_5 . (c) S_6 .
Note: In Fig. 13, $V_{GS_{S1}}$, $V_{GS_{S5}}$, $V_{GS_{S6}}$ are the gate-source of S_1 , S_5 , S_6 ; $V_{DS_{S1}}$, $V_{DS_{S5}}$, $V_{DS_{S6}}$ are the drain-source voltage of S_1 , S_5 , S_6 .

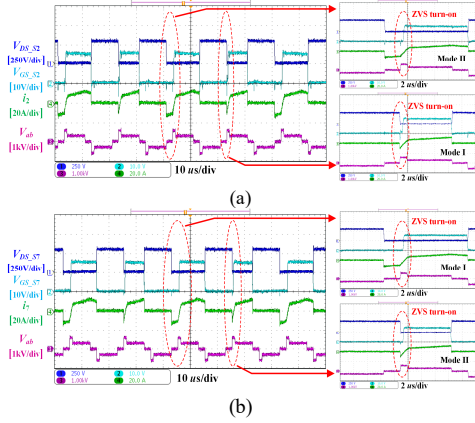


Fig. 14. ZVS achievement performances under working pattern II ($V_{in} = 550$ V, $V_o = 50$ V, $P_o = 1.5$ kW). (a) S_2 . (b) S_7 .
Note: In Fig. 14, $V_{GS_{S2}}$, $V_{GS_{S7}}$ are the gate-source voltage of S_2 , S_7 ; $V_{DS_{S2}}$, $V_{DS_{S7}}$ are the drain-source voltage of S_2 , S_7 .

Figs. 15 - 17 present the experimental results about the clamping diode currents i_{D9} , i_{D10} , i_{D11} , i_{D12} , outer switch currents i_1 , i_4 , i_5 , i_8 , and inner switch currents i_2 , i_3 , i_6 , i_7 , respectively, under the DPS strategy and proposed strategy.

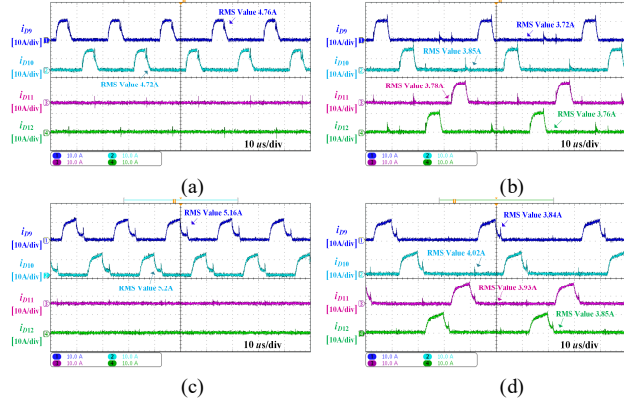


Fig. 15. Experimental results of clamping diode currents i_{D9} , i_{D10} , i_{D11} , and i_{D12} ($V_o = 50$ V, $P_o = 1.5$ kW). (a) Three-level mode of DPS strategy ($V_{in} = 350$ V). (b) Working pattern I of proposed strategy ($V_{in} = 350$ V). (c) Two-level mode of DPS strategy ($V_{in} = 550$ V). (d) Working pattern II of proposed strategy ($V_{in} = 550$ V).

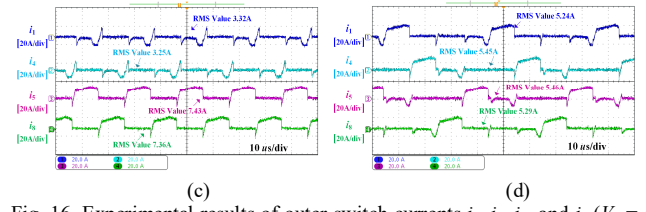
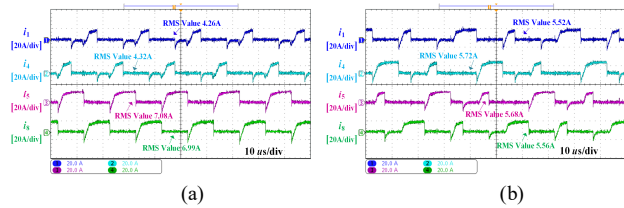


Fig. 16. Experimental results of outer switch currents i_1 , i_4 , i_5 , and i_8 ($V_o = 50$ V, $P_o = 1.5$ kW). (a) Three-level mode of DPS strategy ($V_{in} = 350$ V). (b) Working pattern I of proposed strategy ($V_{in} = 350$ V). (c) Two-level mode of DPS strategy ($V_{in} = 550$ V). (d) Working pattern II of proposed strategy ($V_{in} = 550$ V).

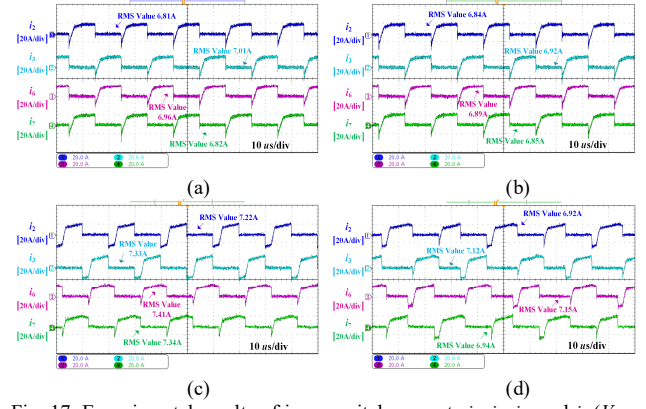


Fig. 17. Experimental results of inner switch currents i_2 , i_3 , i_6 , and i_7 ($V_o = 50$ V, $P_o = 1.5$ kW). (a) Three-level mode of DPS strategy ($V_{in} = 350$ V). (b) Working pattern I of proposed strategy ($V_{in} = 350$ V). (c) Two-level mode of DPS strategy ($V_{in} = 550$ V). (d) Working pattern II of proposed strategy ($V_{in} = 550$ V).

From Figs. 15 - 17, it can be observed that: 1) the clamping diode currents i_{D9} , i_{D10} , i_{D11} , i_{D12} , the outer switch currents i_1 , i_4 , i_5 , i_8 , and inner switch currents i_2 , i_3 , i_6 , i_7 are unbalanced under the DPS strategy; but 2) by utilizing the proposed strategy, the clamping diode currents i_{D9} , i_{D10} , i_{D11} , i_{D12} , the outer switch currents i_1 , i_4 , i_5 , i_8 , and inner switch currents i_2 , i_3 , i_6 , i_7 can be balanced; 3) the experimental results shown in Figs. 15 - 17 are consistent with the theoretical analysis in Section II and IV-D.

Fig. 18 shows the experimental results about transition performance between the two working patterns, which includes the input voltage (V_{in}), voltages on the two input capacitors (V_1 , V_2), and ac component of the output voltage V_o . In Fig. 18, the input voltage steps up from 300 V to 550 V and is finally set back to 300 V when the output voltage V_o is 50 V and output power P_o is 1.5 kW. From Fig. 18, it can be observed that there is no abnormal voltage spike on the two input capacitors during the transitions between the two working patterns.

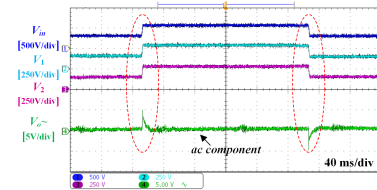


Fig. 18. Experimental results about transition performance between two working patterns when $V_o = 50$ V and $P_o = 1.5$ kW.

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Normally, the conduction power loss and thermal stress on the power device is closely related to the current flowing through it. Figs. 19 and 20 present the comparison results about the loss breakdown and thermal stresses of the primary power devices between the conventional strategy and proposed strategy, respectively.

From Fig. 19, it can be observed that: 1) under the DPS strategy, the conduction losses among the inner power switches are balanced because the RMS values of the currents through the inner power switches are almost the same and MOSFET is used for the primary power switches in the built prototype, but the conduction losses among the outer power switches and clamping diodes are unbalanced; 2) after utilizing the proposed strategy, the conduction losses among the outer power switches, inner power switches, and clamping diodes become balanced. It needs to be mentioned that: if IGBT is used for the power switches, the conduction losses among the inner power switches would become unbalanced under the conventional strategy because the average values of the currents through the inner power switches are different. These power loss imbalances under the conventional strategy would result in the thermal stress imbalance among the primary power devices as shown in Fig. 20. Under the DPS strategy, the thermal stress of D_9, D_{10} are higher than that of D_{11}, D_{12} and the thermal stress of $(S_1, D_1), (S_4, D_4)$ are lower than that of other power switches as shown in Figs. 20(a) and 20(c), which means that the thermal stresses among the power switches and clamping diodes are unbalanced. After utilizing the proposed strategy, the thermal stresses among the clamping diodes $D_9 - D_{12}$, outer power switches $(S_1, D_1), (S_4, D_4), (S_5, D_5), (S_8, D_8)$, and inner power switches $(S_2, D_2), (S_3, D_3), (S_6, D_6), (S_7, D_7)$ become balanced as shown in Figs. 20(b) and 20(d).

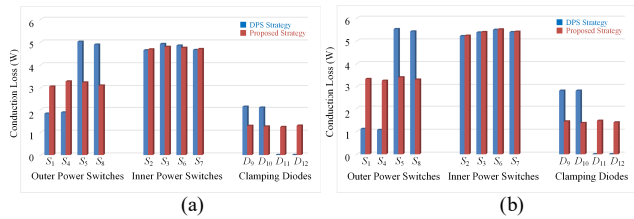


Fig. 19. Loss breakdown of primary power devices ($V_o = 50$ V and $P_o = 1.5$ kW). (a) Working pattern I ($V_{in} = 350$ V). (b) Working Pattern II ($V_{in} = 550$ V).

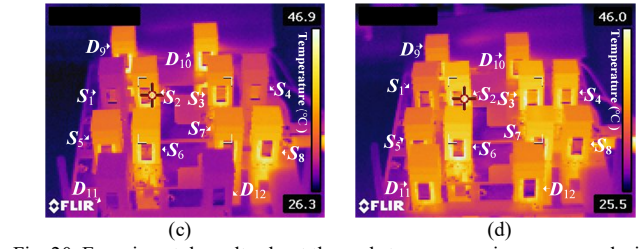
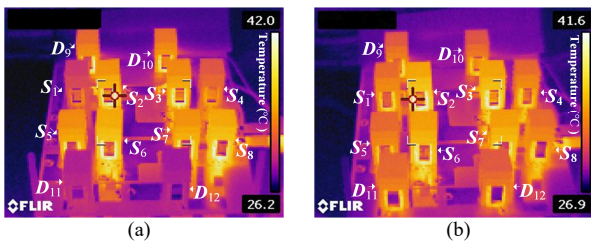


Fig. 20. Experimental results about thermal stresses on primary power devices by FLIR thermal camera. ($V_o = 50$ V, $P_o = 1.5$ kW, Ambient temperature = 25°C). (a) Three-level mode of DPS strategy ($V_{in} = 350$ V). (b) Working pattern I of proposed strategy ($V_{in} = 350$ V). (c) Two-level mode of DPS strategy ($V_{in} = 550$ V). (d) Working pattern II of proposed strategy ($V_{in} = 550$ V).

Fig. 21 shows the experimental comparison results about efficiencies between the conventional strategy and proposed strategy. From Fig. 21, it can be observed that: 1) the efficiencies under the working pattern I of the proposed strategy are almost the same as that under the three-level mode of the DPS strategy; 2) the efficiencies under the working pattern II of the proposed strategy are slightly lower than that under the three-level mode of the DPS strategy. Fig. 22 presents the loss breakdown of main components in the FBTL DC/DC converter under the conventional DPS strategy and proposed strategy when P_o is 1.5 kW. From Fig. 22, it can be observed that: 1) the conduction losses of the primary power switches under the DPS strategy and proposed strategy are almost the same; 2) the DPS and proposed strategy both realize ZVS, and the switching-off losses are almost the same, so the switching losses of the primary power switches would be almost the same; 3) the power losses of the transformer under the two strategies would be almost the same because the primary voltage and primary voltage on the transformer are almost the same; 4) the secondary components' power losses would be almost the same because the secondary voltage and current are almost the same.

It needs to be mentioned that: with the decreasing of the output power, the conduction losses of the primary power devices under the working pattern I of proposed strategy and three-level mode of DPS strategy are almost the same, but the conduction losses of the primary power devices under the working pattern II of proposed strategy become higher than that under the two-level mode of DPS strategy, which results in that the converter's efficiencies under the working pattern II become lower than that under the two-level mode with the decreasing of the output power as shown in Fig. 21. The reason causing lower efficiencies is that MOSFET is used for the power switches in the established prototype. When using MOSFET, the primary current i_p flows through the two body diodes of the power switches instead of the power switches themselves during the free-wheeling time periods (as $[t_5 - t_6]$, $[t_9 - t_{10}]$, $[t_{13} - t_{14}]$, and $[t_{17} - t_{18}]$ in Fig. 5(b)) under the working pattern II of proposed strategy. With the decreasing of the output power, the free-wheeling time periods would become longer, which would thus increase the conduction losses in comparison with the DPS strategy because the conduction loss of power switch is lower than that of its body diode when the same current flows through them [27]. However, when IGBT

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is used for the power switches to satisfy the higher voltage and power applications, the primary current i_p would both flow through the two power switches and two body diodes during the free-wheeling time periods under the two-level mode and working pattern II.

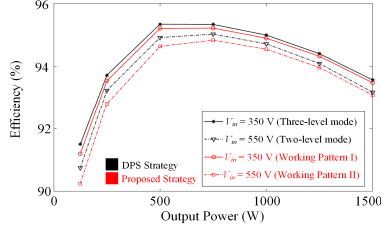
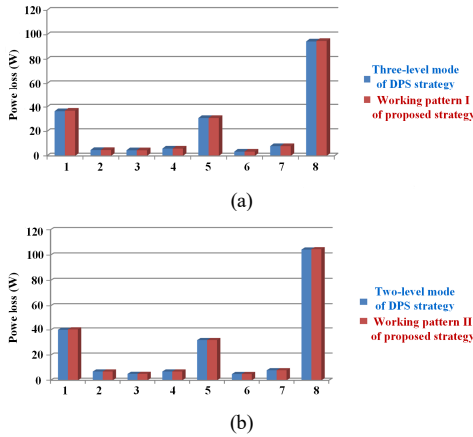


Fig. 21. Experimental comparison results about efficiencies.



Note: 1. Primary power devices' conduction loss. 2. Primary power switches' switching loss. 3. Transformer's core loss. 4. Transformer's copper loss. 5. Output rectifier diodes' loss. 6. Output filter inductor's loss. 8. PCB loss. 10. Total loss.

Fig. 22. Comparison results about loss breakdown when $V_o = 50$ V, and $P_o = 1.5$ kW. (a) $V_{in} = 350$ V. (b) $V_{in} = 550$ V.

VI. CONCLUSION

This paper points out that there exists the current imbalance issue of primary power devices under the conventional strategies in the FBTL DC/DC converter based on the detailed analysis. Then, in order to eliminate these current imbalances, a new modulation strategy is proposed for the FBTL DC/DC converter. In addition, the proposed strategy is composed of two working patterns, which can not only realize zero-voltage switching (ZVS) but also satisfy the wide input voltage range. The transition between these two working patterns is seamless. More significantly, these two working patterns of the proposed strategy can both effectively balance the currents among power switches and clamping diodes, which would thus improve the reliability of the FBTL DC/DC converter by balancing the thermal stresses among the power switches and clamping diodes. Finally, a 1.5 kW experimental prototype is established, and the experimental results verify that the current difference and thermal stress difference among the inner power switches, outer power switches, and clamping diodes are almost zero under the proposed strategy.

APPENDIX

See Table V.

TABLE V. PARAMETERS OF EXPERIMENTAL PROTOTYPE

Component	Description
Power Switches $S_1 - S_4$	SPW47N60C3
Power Diodes $D_1 - D_8$	DSEI30-10AR
Rectifier Diodes $D_{r1} - D_{r4}$	MBR40250TG
Turns Ratio of Transformer T_r ($n : 1$)	25 : 8
Added inductor plus Leakage Inductor L_r (μ H)	47.7
Input Capacitors C_1 and C_2 (μ F)	470
Flying Capacitors C_{s1} and C_{s2} (μ F)	47
Output Filter Capacitor C_o (μ F)	470
Output Filter Inductor L_o (μ H)	140
Switching Frequency (kHz)	50

The derivation of the current expressions in Table IV are presented as below based on Fig. 5.

1) Under working pattern I:

$$\begin{aligned}
 i_{1_rms_I} = i_{4_rms_I} = i_{5_rms_I} = i_{8_rms_I} &= \sqrt{\frac{2 \cdot \int_0^{\frac{2L_r I_o}{n^2 V_{in}}} \left(\frac{V_{in}}{L_r} \cdot t - \frac{I_o}{n} \right)^2 \cdot dt + \int_0^{\frac{T_s}{2}} \frac{2L_r I_o}{n^2 V_{in}} \left(\frac{I_o}{n} \right)^2 \cdot dt + \int_0^{d_1 T_s} \frac{2L_r I_o}{n^2 V_{in}} \left(\frac{I_o}{n} \right)^2 \cdot dt}{2 \cdot T_s}} = \sqrt{\frac{I_o^2 \cdot (1 + 2 \cdot d_1)}{4 \cdot n^2} - \frac{4 \cdot L_r \cdot I_o^3}{3 \cdot V_{in} \cdot n^3 \cdot T_s}} \\
 i_{1_avg_I} = i_{4_avg_I} = i_{5_avg_I} = i_{8_avg_I} &= \frac{2 \cdot \int_0^{\frac{2L_r I_o}{n^2 V_{in}}} \left(\frac{V_{in}}{L_r} \cdot t - \frac{I_o}{n} \right) \cdot dt + \int_0^{\frac{T_s}{2}} \frac{2L_r I_o}{n^2 V_{in}} \left(\frac{I_o}{n} \right) \cdot dt + \int_0^{d_1 T_s} \frac{2L_r I_o}{n^2 V_{in}} \left(\frac{I_o}{n} \right) \cdot dt}{2 \cdot T_s} = \frac{I_o \cdot (1 + 2 \cdot d_1)}{4 \cdot n} - \frac{2 \cdot L_r \cdot I_o^2}{V_{in} \cdot n^2 \cdot T_s} \\
 i_{2_rms_I} = i_{3_rms_I} = i_{6_rms_I} = i_{7_rms_I} &= \sqrt{\frac{2 \cdot \int_0^{\frac{2L_r I_o}{n^2 V_{in}}} \left(\frac{V_{in}}{L_r} \cdot t - \frac{I_o}{n} \right)^2 \cdot dt + 2 \cdot \int_0^{\frac{T_s}{2}} \frac{2L_r I_o}{n^2 V_{in}} \left(\frac{I_o}{n} \right)^2 \cdot dt}{2 \cdot T_s}} = \sqrt{\frac{I_o^2}{2 \cdot n^2} - \frac{4 \cdot L_r \cdot I_o^3}{3 \cdot V_{in} \cdot n^3 \cdot T_s}} \\
 i_{2_avg_I} = i_{3_avg_I} = i_{6_avg_I} = i_{7_avg_I} &= \frac{2 \cdot \int_0^{\frac{2L_r I_o}{n^2 V_{in}}} \left(\frac{V_{in}}{L_r} \cdot t - \frac{I_o}{n} \right) \cdot dt + 2 \cdot \int_0^{\frac{T_s}{2}} \frac{2L_r I_o}{n^2 V_{in}} \left(\frac{I_o}{n} \right) \cdot dt}{2 \cdot T_s} = \frac{I_o}{2 \cdot n} - \frac{2 \cdot L_r \cdot I_o^2}{V_{in} \cdot n^2 \cdot T_s}
 \end{aligned}$$

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$$i_{D9_rms_I} = i_{D10_rms_I} = i_{D11_rms_I} = i_{D12_rms_I} = \sqrt{\frac{\int_0^{\frac{T_s}{2}-d_1T_s} \left(\frac{I_o}{n}\right)^2 dt}{2 \cdot T_s}} = \frac{I_o}{n} \cdot \sqrt{\frac{1-2 \cdot d_1}{4}}$$

$$i_{D9_avg_I} = i_{D10_avg_I} = i_{D11_avg_I} = i_{D12_avg_I} = \frac{\int_0^{\frac{T_s}{2}-d_1T_s} \left(\frac{I_o}{n}\right) dt}{2 \cdot T_s} = \frac{I_o \cdot (1-2 \cdot d_1)}{4 \cdot n}$$

2) Under working pattern II:

$$i_{1_rms_II} = i_{4_rms_II} = i_{5_rms_II} = i_{8_rms_II} = \sqrt{\frac{2 \cdot \int_0^{\frac{t_r \cdot I_o}{n \cdot V_{in}}} \left(\frac{V_{in}}{L_r} \cdot t - \frac{I_o}{n}\right)^2 \cdot dt + \int_0^{\frac{2 \cdot t_r \cdot I_o}{n \cdot V_{in}}} \left(\frac{V_{in}}{2 \cdot L_r} \cdot t\right)^2 \cdot dt + \int_0^{\frac{T_s}{2}} \frac{3 \cdot t_r \cdot I_o}{n \cdot V_{in}} \left(\frac{I_o}{n}\right)^2 \cdot dt + \int_0^{\frac{T_s}{2}-d_2T_s} \left(\frac{I_o}{n}\right)^2 \cdot dt}{2 \cdot T_s}}$$

$$= \sqrt{\frac{I_o^2 \cdot (1-d_2)}{2 \cdot n^2} - \frac{5 \cdot L_r \cdot I_o^3}{6 \cdot V_{in} \cdot n^3 \cdot T_s}}$$

$$i_{1_avg_II} = i_{4_avg_II} = i_{5_avg_II} = i_{8_avg_II} = \frac{2 \cdot \int_0^{\frac{t_r \cdot I_o}{n \cdot V_{in}}} \left(\frac{V_{in}}{L_r} \cdot t - \frac{I_o}{n}\right) \cdot dt + \int_0^{\frac{2 \cdot t_r \cdot I_o}{n \cdot V_{in}}} \left(\frac{V_{in}}{2 \cdot L_r} \cdot t\right) \cdot dt + \int_0^{\frac{T_s}{2}} \frac{3 \cdot t_r \cdot I_o}{n \cdot V_{in}} \left(\frac{I_o}{n}\right) \cdot dt + \int_0^{\frac{T_s}{2}-d_2T_s} \left(\frac{I_o}{n}\right) \cdot dt}{2 \cdot T_s} = \frac{I_o \cdot d_2}{2 \cdot n} - \frac{3 \cdot L_r \cdot I_o^2}{2 \cdot V_{in} \cdot n^3 \cdot T_s}$$

$$i_{2_rms_II} = i_{3_rms_II} = i_{6_rms_II} = i_{7_rms_II} = \sqrt{\frac{2 \cdot \int_0^{\frac{t_r \cdot I_o}{n \cdot V_{in}}} \left(\frac{V_{in}}{L_r} \cdot t - \frac{I_o}{n}\right)^2 \cdot dt + 2 \cdot \int_0^{\frac{2 \cdot t_r \cdot I_o}{n \cdot V_{in}}} \left(\frac{V_{in}}{2 \cdot L_r} \cdot t\right)^2 \cdot dt + \int_0^{\frac{T_s}{2}} \frac{3 \cdot t_r \cdot I_o}{n \cdot V_{in}} \left(\frac{I_o}{n}\right)^2 \cdot dt + \int_0^{\frac{T_s}{2}-d_2T_s} \left(\frac{I_o}{n}\right)^2 \cdot dt + \int_0^{d_2T-\frac{3 \cdot t_r \cdot I_o}{n \cdot V_{in}}} \left(\frac{I_o}{n}\right)^2 \cdot dt}{2 \cdot T_s}}$$

$$= \sqrt{\frac{I_o^2}{2 \cdot n^2} - \frac{2 \cdot L_r \cdot I_o^3}{V_{in} \cdot n^3 \cdot T_s}}$$

$$i_{2_avg_II} = i_{3_avg_II} = i_{6_avg_II} = i_{7_avg_II} = \frac{2 \cdot \int_0^{\frac{t_r \cdot I_o}{n \cdot V_{in}}} \left(\frac{V_{in}}{L_r} \cdot t - \frac{I_o}{n}\right) \cdot dt + 2 \cdot \int_0^{\frac{2 \cdot t_r \cdot I_o}{n \cdot V_{in}}} \left(\frac{V_{in}}{2 \cdot L_r} \cdot t\right) \cdot dt + \int_0^{\frac{T_s}{2}} \frac{3 \cdot t_r \cdot I_o}{n \cdot V_{in}} \left(\frac{I_o}{n}\right) \cdot dt + \int_0^{\frac{T_s}{2}-d_2T_s} \left(\frac{I_o}{n}\right) \cdot dt + \int_0^{d_2T-\frac{3 \cdot t_r \cdot I_o}{n \cdot V_{in}}} \left(\frac{I_o}{n}\right) \cdot dt}{2 \cdot T_s}$$

$$= \frac{I_o \cdot d_2}{n} - \frac{5 \cdot L_r \cdot I_o^2}{2 \cdot V_{in} \cdot n^2 \cdot T_s}$$

$$i_{D9_rms_II} = i_{D10_rms_II} = i_{D11_rms_II} = i_{D12_rms_II} = \sqrt{\frac{\int_0^{\frac{2 \cdot t_r \cdot I_o}{n \cdot V_{in}}} \left(\frac{V_{in}}{2 \cdot L_r} \cdot t\right)^2 \cdot dt + \int_0^{d_2T-\frac{3 \cdot t_r \cdot I_o}{n \cdot V_{in}}} \left(\frac{I_o}{n}\right)^2 \cdot dt}{2 \cdot T_s}} = \sqrt{\frac{I_o^2 \cdot d_2}{2 \cdot n^2} - \frac{7 \cdot L_r \cdot I_o^3}{6 \cdot V_{in} \cdot n^3 \cdot T_s}}$$

$$i_{D9_avg_II} = i_{D10_avg_II} = i_{D11_avg_II} = i_{D12_avg_II} = \frac{\int_0^{\frac{2 \cdot t_r \cdot I_o}{n \cdot V_{in}}} \left(\frac{V_{in}}{2 \cdot L_r} \cdot t\right) \cdot dt + \int_0^{d_2T-\frac{3 \cdot t_r \cdot I_o}{n \cdot V_{in}}} \left(\frac{I_o}{n}\right) \cdot dt}{2 \cdot T_s} = \frac{I_o \cdot d_2}{2 \cdot n} - \frac{L_r \cdot I_o^2}{V_{in} \cdot n^3 \cdot T_s}$$

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